Assignment #3

FPGA Based System Design (Spring 2013)

Electronics Engineering Department

Sub-Campus Chakwal

Problem 1.

Draw the State Diagram of sequence detector which detects the first letter of your name and write Verilog code of the state diagram along with testbench.

Alphabet	Encoding
A	00000
B	00001
C	00010
D	00011
E	00100
F	00101
G	00110
H	00111
I	01000
G	01001
K	01010
L	01011
M	01100
N	01101
O	01110
P	01111
Q	10000
R	10001
S	10010
T	10011
U	10100
V	10101
W	10110
X	10111
Y	11000
Z	11001

Note:

i. *Each Assignment submitted should have title page which should include Assignment number, Your Name, Reg. No, Section, Subject Name, Teachers Name and Date.*